

## CLAIMS

What is claimed is:

1. An interconnect for transporting, within a network node, data between a primary circuit component and a secondary circuit component, the interconnect  
5 comprising:
  - (a) primary to\_mate transmitting means, including a buffer for storing data to be transmitted over the interconnect, and a transmit controlling means for controlling the insertion of control characters into the data to be transmitted;
  - 10 (b) primary from\_mate receiving means, including a buffer for storing received data, and a receive controlling means for interpreting control characters inserted into the data;
  - (c) secondary to\_mate transmitting means, including a buffer for storing data to be transmitted over the interconnect, and a transmit controlling means  
15 for controlling the insertion of control characters into the data stream to be transmitted;
  - (d) secondary from\_mate receiving means, including a buffer for storing received data, and a receive controlling means for interpreting the control characters inserted into the data;
  - 20 (e) first linking means for communicating data between the primary to\_mate transmitting means and the secondary from\_mate receiving means;
  - (f) second linking means for communicating data between the secondary to\_mate transmitting means and the primary from\_mate receiving means, the second linking means operating distinctly from the first linking  
25 means such that data may be transmitted at the same time over the first linking means and the second linking means;
  - (g) whereby the transmit controlling means in the primary to\_mate transmitting means is connected with the receive controlling means in the

primary from<sub>\_mate</sub> receiving means, and the transmit controlling means in the secondary to<sub>\_mate</sub> transmitting means is connected with the receive controlling means in the secondary from<sub>\_mate</sub> receiving means, such that when a receive controlling means in the respective from<sub>\_mate</sub> receiving means detects that the fill level of the receive buffer is above a threshold, the corresponding to<sub>\_mate</sub> transmit controlling means inserts a transmit off (XOFF) control character in the data, and when the receive controlling means in the respective from<sub>\_mate</sub> receiving means detects a transmit off (XOFF), the corresponding to<sub>\_mate</sub> transmitting means stops transmitting data; and

(h) whereby the transmit controlling means in the primary to<sub>\_mate</sub> transmitting means is connected with the receive controlling means in the primary from<sub>\_mate</sub> receiving means, and the transmit controlling means in the secondary to<sub>\_mate</sub> transmitting means is connected with the receive controlling means in the secondary from<sub>\_mate</sub> receiving means, such that when the receive controlling means in the respective from<sub>\_mate</sub> receiving means detects that the fill level of the receive buffer is below a threshold, the corresponding to<sub>\_mate</sub> transmit controlling means inserts a transmit on (XON) control character , and when the receive controlling means in the respective from<sub>\_mate</sub> receiving means detects a XON control character, the corresponding to<sub>\_mate</sub> transmitting means is enabled to transmit data.

2. An apparatus as in claim 1 wherein the transmit controlling means in the primary to<sub>\_mate</sub> transmitting means is connected with the receive controlling means in the primary from<sub>\_mate</sub> receiving means, and the transmit controlling means in the secondary to<sub>\_mate</sub> transmitting means is connected with the receive controlling means in the secondary from<sub>\_mate</sub> receiving means, such that when the receive controlling means in the respective from<sub>\_mate</sub> receiving means

detects an Out of Sync (OOS) indication, the corresponding to\_mate transmit controlling means inserts a synchronization sequence (SYNC\_OOS) until the OOS indication is no longer detected by the from\_mate receiving means.

3. An apparatus as in claim 1 wherein each of the first and second linking means  
5 additionally comprise multiple parallel circuit paths over which data can be simultaneously transmitted and received.
4. An apparatus as in claim 1 wherein each transmit controlling means comprises a timer to ensure that the control characters XON, XOFF, and OOS are inserted at regular intervals during the transmission of a packet.
- 10 5. An apparatus as in claim 1 wherein the data is encoded with an 8-bit to 10-bit encoder and the control characters are encoded with 10-bit code words which are not assigned to encode data symbols.
6. An apparatus as in claim 1 wherein the primary and secondary circuit components are located on different circuit boards.
- 15 7. An apparatus as in claim 1 wherein:
  - (i) the primary to\_mate transmitting means is connected to the secondary from\_mate receiving means to permit data to be passed through between them, and the secondary to-mate transmitting means is connected to the primary from\_mate receiving means to permit data to be passed through  
20 between them, and wherein pass-through connection status information is encoded onto the control characters.
8. An apparatus as in claim 7 wherein the pass-through connection status information is encoded into the XON or XOFF control characters.

9. An interconnect for transporting data between a primary circuit component and a secondary circuit component, the interconnect comprising:
- 5 (a) primary to\_mate transmitting means, including a buffer for storing data to be transmitted over the interconnect, and a transmit controlling means for controlling the insertion of control characters into the data to be transmitted;
  - (b) primary from\_mate receiving means, including a buffer for storing received data, and a receive controlling means for interpreting control characters inserted into the data;
  - 10 (c) secondary to\_mate transmitting means, including a buffer for storing data to be transmitted over the interconnect, and a transmit controlling means for controlling the insertion of control characters into the data stream to be transmitted;
  - (d) secondary from\_mate receiving means, including a buffer for storing  
15 received data, and a receive controlling means for interpreting the control characters inserted into the data;
  - (e) first link means for communicating data between the primary to\_mate transmitting means and the secondary from\_mate receiving means;
  - (f) second linking means for communicating data between the secondary  
20 to\_mate transmitting means and the primary from\_mate receiving means, the second linking means operating distinctly from the first linking means such that data may be transmitted at the same time over the first linking means and the second linking means;
  - (g) whereby the transmit controlling means in the primary to\_mate  
25 transmitting means is connected with the receive controlling means in the primary from\_mate receiving means, and the transmit controlling means in the secondary to\_mate transmitting means is connected with the receive controlling means in the secondary from\_mate receiving means, such that when a receive controlling means in the respective from\_mate

5 receiving means detects that the fill level of the receive buffer is above a threshold, the corresponding to \_mate transmit controlling means inserts a transmit off (XOFF) control character in the data, and when the receive controlling means in the respective from \_mate receiving means detects a transmit off (XOFF), the corresponding to \_mate transmitting means stops transmitting data;

10 (h) whereby the transmit controlling means in the primary to \_mate transmitting means is connected with the receive controlling means in the primary from \_mate receiving means, and the transmit controlling means in the secondary to \_mate transmitting means is connected with the receive controlling means in the secondary from \_mate receiving means, such that when the receive controlling means in the respective from \_mate receiving means detects that the fill level of the receive buffer is below a threshold, the corresponding to \_mate transmit controlling means inserts a transmit on (XON) control character, and when the receive controlling means in the respective from \_mate receiving means detects a XON control character, the corresponding to \_mate transmitting means is enabled to transmit data; and

15 (i) the primary to \_mate transmitting means is connected to the secondary from \_mate receiving means to permit data to be passed through between them, and the secondary to-mate transmitting means is connected to the primary from \_mate receiving means to permit data to be passed through between them, and wherein the pass-through connection status information is encoded into an end of packet control character.

25 10. An apparatus as in claim 9 wherein the transmit controlling means in the primary to \_mate transmitting means is connected with the receive controlling means in the primary from \_mate receiving means, and the transmit controlling means in the secondary to \_mate transmitting means is connected with the receive

controlling means in the secondary from\_mate receiving means, such that when the receive controlling means in the respective from\_mate receiving means detects an Out of Sync (OOS) indication, the corresponding to\_mate transmit controlling means inserts a synchronization sequence (SYNC\_OOS) until the  
5 OOS indication is no longer detected by the from\_mate receiving means.

11. An apparatus as in claim 9 wherein each of the first and second linking means additionally comprise multiple parallel circuit paths over which data can be simultaneously transmitted and received.
12. An apparatus as in claim 9 wherein each transmit controlling means comprises a  
10 timer to ensure that the control characters XON, XOFF, and OOS are inserted at regular intervals during the transmission of a packet.
13. An apparatus as in claim 9 wherein the data is encoded with an 8-bit to 10-bit encoder and the control characters are encoded with 10-bit code words which are not assigned to encode data symbols.
- 15 14. An apparatus as in claim 9 wherein the primary and secondary circuit components are located on different circuit boards.
15. An apparatus for transporting data between a first internetworking device and a second internetworking device, comprising:  
a pair of ring connecting means for coupling the first and second  
20 internetworking devices together, such that data packets travel along an outer ring direction from the first internetworking device to the second internetworking device, and such that data packets also travel along an inner ring direction from the second internetworking device to the first internetworking device;

- first and second ring access control means, associated with each of the first and second internetworking devices, each ring access controlling means for receiving data from a respective one internetworking device on a respective ring, and for transmitting data from the internetworking device onto the other ring, the ring access controlling means also for connecting pass-through data packets along a pair of forwarding paths, the forwarding paths including an outer forwarding path for forwarding pass-through data packets received from an outer ring input connection serviced by the first ring access controlling means to an outer ring output connection serviced by the second ring access controlling means, and the forwarding paths also including an inner forwarding path for forwarding pass-through data packets receiving from an inner ring input connection serviced by the second ring access controlling means to an inner ring transmit connection serviced by the first ring access controlling means; and wherein each of the ring access control means embed control characters in the data packets transmitted over the inner forward path and the outer forward path, the control characters indicating pass-through control information for the respective data packet in the same control character as used for synchronization.
16. An apparatus as in claim 15 wherein the control characters that indicate pass-through control information also indicate flow control status.
17. An apparatus as in claim 15 wherein a SYNC control character sequence is assigned for a SYNC-XON state in which the flow control is transmit on with no pass-through, a SYNC-XOFF state in which the flow control is transmit off with no pass-through, a SYNC-XON-PASS state in which the flow control is transmit on with pass-through, and a SYNC-XOFF-PASS state in which the flow control is transmit off with pass-through.

18. An apparatus as in claim 15 wherein the data packets are encoded using an 8-bit to 10-bit code, wherein the 10-bit code words not assigned to data are used for the control characters.
19. An apparatus as in claim 15 wherein the inner forward link and outer forward link are implemented using a plurality of individual parallel data busses, and wherein a plurality of data bytes comprising a packet are forwarded over the plurality of links together and in parallel, with any unused data bytes in a packet being replaced with idle control characters.
20. An apparatus for transporting data between a first internetworking device and a second internetworking device, comprising:  
a pair of ring connecting means for coupling the first and second internetworking devices together, such that data packets travel along an outer ring direction from the first internetworking device to the second internetworking device, and such that data packets also travel along an inner ring direction from the second internetworking device to the first internetworking device;  
first and second ring access control means, associated with each of the first and second internetworking devices, each ring access control means for receiving data from a respective one internetworking device on a respective ring, and for transmitting data from the internetworking device onto the other ring, the ring access control means also for connecting pass-through data packets along a pair of forwarding paths, the forwarding paths including an outer forwarding path for forwarding pass-through data packets received from an outer ring input connecting means serviced by the first ring access controlling means to an outer ring output connecting means serviced by the second ring access control means, and the forwarding paths also including an inner forwarding path for forwarding pass-through data packets receiving from an inner ring input connecting means

served by the second ring access controlling means to an inner ring transmit connection serviced by the first ring access controlling means; and

5            wherein each of the ring access controlling means embed control characters in the data packets transmitted over the inner forward path and the outer forward path, an end of packet control character indicating pass-through control information for the respective data packet and being used for synchronization.

21.    An apparatus as in claim 20 wherein the control characters that indicate pass-through control information also indicate flow control status.
- 10    22.    An apparatus as in claim 21 wherein a SYNC control character sequence is assigned for a SYNC-XON state in which the flow control is transmit on with no pass-through, a SYNC-XOFF state in which the flow control is transmit off with no pass-through, a SYNC-XON-PASS state in which the flow control is transmit on with pass-through, and a SYNC-XOFF-PASS state in which the flow control
- 15    is transmit off with pass-through.
23.    An apparatus as in claim 20 wherein the data packets are encoded using an 8-bit to 10-bit code, wherein the 10-bit code words not assigned to data are used for the control characters.
24.    An apparatus as in claim 20 wherein the inner forward link and outer forward
- 20    link are implemented using a plurality of individual parallel data busses, and wherein a plurality of data bytes comprising a packet are forwarded over the plurality of links together and in parallel, with any unused data bytes in a packet being replaced with idle control characters.
25.    A computer program product comprising:

a computer usable medium for transporting data across an interconnect between a primary circuit component and a secondary circuit component;

a set of computer program instructions embodied on the computer usable medium, including instructions to:

- 5       (a)     in a primary to\_mate transmitter,  
              store, in a buffer, data to be transmitted over the  
              interconnect, and  
              control, in a transmit controller, the insertion of control  
              characters into the data to be transmitted;
- 10       (b)     in a primary from\_mate receiver,  
              store, in a buffer, received data, and  
              interpret, in a receive controller, control characters  
              inserted into said received data;
- 15       (c)     in a secondary to\_mate transmitter,  
              store, in a buffer, data to be transmitted over the  
              interconnect, and  
              control, in a transmit controller, the insertion of control  
              characters into the data stream to be transmitted;
- 20       (d)     in a secondary from\_mate receiver,  
              store, in a buffer, received data, and  
              interpret, in a receive controller, control characters  
              inserted into said received data;
- 25       (e)     communicate, over a first link, data between the primary to\_mate  
              transmitter and the secondary from\_mate receiver;
- (f)     communicate, over a second link, data between the secondary to\_mate  
              transmitter and the primary from\_mate receiver, the second link  
              operating distinctly from the first link such that data may be transmitted  
              at the same time over the first link and the second link;

- (g) whereby the transmit controller in the primary to\_mate transmitter is connected with the receive controller in the primary from\_mate receiver, and the transmit controller in the secondary to\_mate transmitter is connected with the receive controller in the secondary from\_mate receiver, further comprising instructions to:
- 5 detect, in a receive controller in the respective from\_mate receiver, when the fill level of the receive buffer is above a threshold,
- 10 upon said detection, insert, in the corresponding to\_mate transmit controller, a transmit off (XOFF) control character in the data,
- detect, in the receive controller in the respective from\_mate receiver, a transmit off (XOFF), and
- 15 upon said XOFF detection, stop, in the corresponding to\_mate transmitter, transmission of data;
- (h) whereby the transmit controller in the primary to\_mate transmitter is connected with the receive controller in the primary from\_mate receiver, and the transmit controller in the secondary to\_mate transmitter is connected with the receive controller in the secondary from\_mate receiver, further comprising instructions to:
- 20 detect, in the receive controller in the respective from\_mate receiver, when the fill level of the receive buffer is below a threshold,
- 25 upon said detecting, insert, in the corresponding to\_mate transmit controller, a transmit on (XON) control character,
- detect, in the receive controller in the respective from\_mate receiver, a XON control character, and
- enable, in the corresponding to\_mate transmitter, transmission of data; and

- (i) whereby the primary to\_mate transmitter is connected to the secondary from\_mate receiver to permit data to be passed through between them, and the secondary to\_mate transmitter is connected to the primary from\_mate receiver to permit data to be passed through between them, further comprising instructions to:
- 5                    encode the pass-through connection status information into an end of packet control character.
26.    The computer program product of claim 25 wherein the transmit controller in the primary to\_mate transmitter is connected with the receive controller in the primary from\_mate receiver, and the transmit controller in the secondary to\_mate transmitter is connected with the receive controller in the secondary from\_mate receiver, further comprising instructions to:
- 10                    detect, in the receive controller in the respective from\_mate receiver, an Out of Sync (OOS) indication, and
- 15                    upon said detection, insert, in the corresponding to\_mate transmit controller, a synchronization sequence (SYNC\_OOS) until the OOS indication is no longer detected by the from\_mate receiver.
27.    The computer program product of claim 25 wherein each of the first and second links additionally comprise multiple parallel circuit paths over which data can be simultaneously transmitted and received.
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28.    The computer program product of claim 25, further comprising instructions to:
- insert the control characters XON, XOFF, and OOS at regular intervals during the transmission of a packet.
29.    The computer program product of claim 25, further comprising instructions to:
- 25                    encode the data with an 8-bit to 10-bit encoder; and

encode the control characters with 10-bit code words which are not assigned to encode data symbols.

30. The computer program product of claim 25 wherein the primary and secondary circuit components are located on different circuit boards.
- 5 31. A computer program product comprising:
- a computer usable medium for transporting data between a first internetworking device and a second internetworking device, wherein a pair of ring connections couple the first and second internetworking devices together, such that data packets travel along an outer ring direction from the first
- 10 internetworking device to the second internetworking device, and such that data packets also travel along an inner ring direction from the second internetworking device to the first internetworking device;
- a set of computer program instructions embodied on the computer usable medium, including instructions to:
- 15 receive, in each of first and second ring access controllers associated with each of first and second internetworking devices, data from a respective one internetworking device on a respective ring;
- transmit, in each of first and second ring access controllers associated with each of first and second internetworking devices, data from the
- 20 internetworking device onto the other ring;
- wherein the ring access controllers connect pass-through data packets along a pair of forwarding paths, the forwarding paths including an outer forwarding path for forwarding pass-through data packets received from an outer ring input connection serviced by the first ring access controller to an outer ring output connection serviced by the second ring access controller, and the
- 25 forwarding paths also including an inner forwarding path for forwarding pass-through data packets receiving from an inner ring input connection serviced

by the second ring access controller to an inner ring transmit connection serviced by the first ring access controller; and

5 wherein each of the ring access controls embed control characters in the data packets transmitted over the inner forward path and the outer forward path, an end of packet control character indicating pass-through control information for the respective data packet and being used for synchronization.

32. The computer program product of claim 31 wherein the control characters that indicate pass-through control information also indicate flow control status.

10 33. The computer program product of claim 32 wherein a SYNC control character sequence is assigned for a SYNC-XON state in which the flow control is transmit on with no pass-through, a SYNC-XOFF state in which the flow control is transmit off with no pass-through, a SYNC-XON-PASS state in which the flow control is transmit on with pass-through, and a SYNC-XOFF-PASS state in which the flow control is transmit off with pass-through.

15 34. The computer program product of claim 31, further comprising instructions to:  
    encode the data packets using an 8-bit to 10-bit code; and  
    encode the control characters with 10-bit code words not assigned to data.

20 35. The computer program product of claim 31 wherein the inner forward link and outer forward link are implemented using a plurality of individual parallel data busses, further comprising instructions to:  
    forward a plurality of data bytes comprising a packet over the plurality of links together and in parallel, with any unused data bytes in a packet being replaced with idle control characters.